

Claims

What is claimed is:

- 1 1. A microelectronic package array, comprising:
 - 2 a first microelectronic package including a first carrier substrate having a first die
 - 3 side and a first non-die side, a first die electrically coupled to the first die side, and a
 - 4 land pad on the first die side;
 - 5 a second microelectronic package comprising a second carrier substrate having
 - 6 a second die side and a second non-die side, a second die electrically coupled to the
 - 7 second die side, and a bond pad on the second non-die side; and
 - 8 an intermediate substrate having a first side and a second side, the first side
 - 9 being coupled to the first die side of the first carrier substrate and the second side being
 - 10 coupled to the second non-die side of the second carrier substrate.
- 1 2. The microelectronic package array of claim 1, wherein the intermediate substrate
 - 2 further comprises
 - 3 a substantially solid core having a first side and a second side;
 - 4 an adhesive material disposed on the first side and second side of the core; and
 - 5 a conductive riser disposed within the solid core.
- 1 3. The microelectronic package array of claim 2, wherein the intermediate substrate
 - 2 is mechanically bonded to the first die side of the first carrier substrate and the second
 - 3 non-die side of the second carrier substrate by the adhesive material.

1 4. The microelectronic package array of claim 3, wherein the adhesive material is a
2 B-stage polymer.

1 5. The microelectronic package array of claim 3, wherein the core is a C-stage
2 resin.

1 6. The microelectronic package array of claim 5, wherein the C-stage resin is
2 reinforced with a matrix to increase stiffness and control the coefficient of thermal
3 expansion of the intermediate substrate.

1 7. The microelectronic package array of claim 6, wherein the matrix is selected from
2 a group including fiberglass cloth, composite fiber and non-woven fabric.

1 8. The microelectronic package array of claim 2, wherein the conductive riser is
2 electrically coupled to the land pad of the first microelectronic package and the bond
3 pad of the second microelectronic package.

1 9. The microelectronic package array of claim 8, wherein the conductive riser
2 includes a first end and a second end having conductive plating disposed thereon, the
3 first and second ends being electrically bonded to the land pad and the bond pad
4 respectively by the conductive plating.

1 10. The microelectronic package array of claim 9, wherein conductive plating is
2 selected from a group including leaded solder, lead-free solder and tin.

1 11. A system, comprising:
2 a system board;
3 a bus disposed on the system board to facilitate data exchange;
4 a memory configured to store data, the memory disposed on the system board
5 and coupled to the bus;
6 a microelectronic package array disposed on the system board and coupled to
7 the bus, the microelectronic package array comprising:
8 a first microelectronic package including a first carrier substrate having a first die
9 side and a first non-die side, a first die electrically coupled to the first die side, and a
10 land pad on the first die side;
11 a second microelectronic package comprising a second carrier substrate having
12 a second die side and a second non-die side, a second die electrically coupled to the
13 second die side, and a bond pad on the second non-die side; and
14 an intermediate substrate coupled to the first die side of the first carrier substrate and
15 the second non-die side of the second carrier substrate.

1 12. The system of claim 11, wherein the intermediate substrate further comprises
2 a substantially solid core having a first side and a second side;
3 an adhesive material disposed on the first side and second side of the core; and
4 a conductive riser disposed within the solid core.

1 13. The system of claim 12, wherein the intermediate substrate is mechanically
2 bonded to the first die side of the first carrier substrate and the second non-die side of
3 the second carrier substrate by the adhesive material.

1 14. The system of claim 13, wherein the adhesive material is a B-stage polymer.

1 15. The system of claim 13, wherein the core is a C-stage resin.

1 16. The system of claim 15, wherein the C-stage resin is reinforced with a matrix to
2 increase stiffness and control the coefficient of thermal expansion of the intermediate
3 substrate.

1 17. The system of claim 16, wherein the matrix is selected from a group including
2 fiberglass cloth, glass fiber carbon fiber and non-woven fabric.

1 18. The system of claim 12, wherein the conductive riser is electrically coupled to the
2 land pad of the first microelectronic package and the bond pad of the second
3 microelectronic package.

1 19. The system of claim 18, wherein the conductive riser includes a first end and a
2 second end having conductive plating disposed thereon, the first and second ends
3 being electrically bonded to the land pad and the bond pad respectively by the
4 conductive plating.

1 20. The system of claim 19, wherein conductive plating is selected from a group
2 including leaded solder, lead-free solder and tin.

1 21. A method for fabricating a microelectronic package array, comprising:
2 providing a first microelectronic package having a first carrier substrate with a
3 first die side and a first non-die side, and a plurality of land pads disposed on the first
4 die side;
5 providing a second microelectronic package having a second carrier substrate
6 with a second die side and a second non-die side, and a plurality of bond pads disposed
7 on the second non-die side;
8 placing an intermediate substrate having a plurality of conductive risers disposed
9 therein on the first die side of a the first carrier substrate;
10 placing the second carrier substrate on the intermediate substrate with the
11 second non-die side coming in contact with the intermediate substrate;
12 mechanically coupling the intermediate substrate to the first and second carrier
13 substrates; and
14 electrically coupling the plurality of conductive risers with the plurality of land and
15 bond pads.

1 22. The method of claim 21, wherein the method further comprises:
2 placing the microelectronic package array in a vacuum chamber;
3 creating a vacuum in the vacuum chamber;
4 applying heat to the microelectronic package array;

- 5 applying pressure to the microelectronic package array;
- 6 releasing the pressure; and
- 7 cooling the microelectronic package array.

1 23. The method of claim 22, wherein creating a vacuum comprises establishing a
2 pressure of about less than ten kilo Pascals.

1 24. The method of claim 22, wherein applying heat comprises raising the
2 temperature to about between 150 °C and 350 °C.

1 25. The method of claim 22, wherein applying a pressure comprises increasing the
2 pressure to a range between 0.5 mega Pascals and 10 mega Pascals.

1 26. The method of claim 21, wherein the intermediate substrate further includes a
2 core having a first side and a second side, and an adhesive material disposed on the
3 first side and the second side.

1 27. The method of claim 26, wherein the core is a C-Stage resin and the adhesive
2 material is a B-stage polymer.